WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a first basic memory block having a plurality of memory cells arranged in a matrix and having a first storage capacity corresponding to a unit of collective erasure, said collective erasure not allowed in a partial region of said first basic memory block, said partial region of said first basic memory block having a second storage capacity smaller than said first storage capacity;

a plurality of second basic memory blocks provided independent of said first basic memory block, each having a plurality of memory cells arranged in a matrix and each having said second storage capacity, a total storage capacity of said plurality of second basic memory blocks being equal to said first storage capacity; and

an erasure control circuit switching, in accordance with a switching signal, between a first operation of erasing one of said plurality of second basic memory blocks in accordance with an erasure command, and a second operation of erasing said plurality of second basic memory blocks collectively in accordance with said erasure command.

2. The non-volatile semiconductor memory device according to claim 1, wherein at least one of said plurality of second basic memory blocks includes a boot block read at a start of a system in which said non-volatile semiconductor memory device is used.

3. The non-volatile semiconductor memory device according to claim 1, wherein at least one of said plurality of second basic memory blocks includes a memory block for programming data that is expected to be rewritten more frequently than data to be programmed into said first basic memory block.

4. The non-volatile semiconductor memory device according to claim 1, further comprising:

a lead supplying a predetermined fixed potential; and

a pad to switch a polarity of said switch signal with respect to said erasure control circuit,

wherein said erasure control circuit includes a select signal generation circuit setting said switch signal at a first polarity when wire bonding is established between said lead and said pad.

5. The non-volatile semiconductor memory device according to claim 1, wherein said erasure control circuit comprises a switch signal generation circuit providing said switch signal,

said switch signal generation circuit includes a non-volatile storage element to determine said switch signal in accordance with stored contents.

6. The non-volatile semiconductor memory device according to claim 5, wherein said non-volatile storage element is a fuse element determining said switch signal in accordance with absence/presence of connection.

7. The non-volatile semiconductor memory device according to claim 5, wherein said non-volatile storage element has a structure identical to the structure of a non-volatile memory cell included in said first and second basic memory blocks.

8. The non-volatile semiconductor memory device according to claim 1, wherein said erasure control circuit selects said plurality of second basic memory blocks together when a pulse is to be applied collectively to a plurality of non-volatile memory cells in the case of said second operation.

9. The non-volatile semiconductor memory device according to claim 1, wherein said erasure control circuit sequentially selects said plurality of second basic memory blocks, and initiates an erasure operation of a subsequent basic memory block of a selected basic memory block after erasure of said selected basic memory block is completed in the case of said

second operation.

10. The non-volatile semiconductor memory device according to claim 1, wherein said plurality of second basic memory blocks and said first basic memory block are allocated a predetermined address region,

said plurality of second basic memory blocks are arranged at a most significant side of said predetermined address region.

11. The non-volatile semiconductor memory device according to claim 1, wherein said plurality of second basic memory blocks and said first basic memory block are allocated a predetermined address region,

said plurality of second basic memory blocks are arranged at a least significant side of said predetermined address region.

12. The non-volatile semiconductor memory device according to claim 1, further comprising a plurality of third basic memory blocks corresponding to a unit of collective erasure, each third basic memory block having a storage capacity smaller than the storage capacity of said first basic memory block, wherein

said plurality of third basic memory blocks, said plurality of second basic memory blocks, and said first basic memory block are allocated a predetermined address region, and

one of said plurality of second basic memory blocks and said plurality of third basic memory blocks are arranged at a most significant side in said predetermined address region, and the other of said plurality of second basic memory blocks and said plurality of third basic memory blocks are arranged at a least significant side of said predetermined address region.

13. A non-volatile semiconductor memory device comprising:

a first basic memory block having a plurality of memory cells arranged in a matrix and having a first storage capacity corresponding to a unit of collective erasure, said collective erasure not allowed in a partial

region of said first basic memory block, said partial region of said first basic memory block having a second storage capacity smaller than said first storage capacity;

a plurality of second basic memory blocks provided independent of said first basic memory block, each having a plurality of memory cells arranged in a matrix and each having said second storage capacity, a total storage capacity of said plurality of second basic memory blocks being equal to said first storage capacity; and

an erasure control circuit switching, in accordance with a switch signal, between a first operation of erasing one of said plurality of second basic memory blocks in accordance with an erasure command, and a second operation of erasing said first basic memory block in accordance with said erasure command.

14. The non-volatile semiconductor memory device according to claim 13, further comprising:

a lead providing a predetermined fixed potential; and

a pad to switch a polarity of said switch signal with respect to said erasure control circuit,

wherein said erasure control circuit includes a switch signal generation circuit setting said switch signal at a first polarity when wire bonding is established between said lead and said pad.

15. The non-volatile semiconductor memory device according to claim 13, wherein said erasure control circuit includes a switch signal generation circuit providing said switch signal,

said switch signal generation circuit includes a non-volatile storage element to determine said switch signal in accordance with stored content.

16. The non-volatile semiconductor memory device according to claim 15, wherein said non-volatile storage element includes a fuse element determining said switch signal in accordance with absence/presence of connection.

17. The non-volatile semiconductor memory device according to claim 15, wherein said non-volatile storage element has a configuration identical to the configuration of a non-volatile memory cell included in said first and second basic memory blocks.

18. The non-volatile semiconductor memory device according to claim 13, wherein said plurality of second basic memory blocks and said first basic memory block are allocated a predetermined address region,

said plurality of second basic memory blocks are arranged at a most significant side of said predetermined address region.

19. The non-volatile semiconductor memory device according to claim 13, wherein said plurality of second basic memory blocks and said first basic memory block are allocated a predetermined address region,

said plurality of second basic memory blocks are arranged at a most significant side of said predetermined address region.

20. The non-volatile semiconductor memory device according to claim 13, further comprising a plurality of third basic memory blocks corresponding to a unit of collective erasure, each third basic memory block having a storage capacity smaller than the storage capacity of said first basic memory block, wherein

said plurality of third basic memory block, said plurality of second basic memory blocks, and said first basic memory block are allocated a predetermined address region, and

one of said plurality of second basic memory blocks and said plurality of third basic memory blocks are arranged at a most significant side of said predetermined address region, and the other of said plurality of second basic memory blocks and said plurality of third basic memory blocks are arranged at a least significant side of said predetermined address region.